REMARKS:

In response to the Office Action mailed on April 4, 2005, Applicant respectfully submits the following remarks. Claims 1-20 are pending in the application and are currently under rejection.

Claim Rejections 35 USC §102

The Examiner has rejected Claims 1, 2, 13-15 under 35 USC §102(b) as being clearly anticipated by Basso et al. Applicant respectfully traverses this rejection of the claims in light of the following remarks.

The claimed invention is directed to the problem of how an electronic device having an internal voltage regulator integrated within the device, which functions to protect a primary function circuit of the device from elevated voltages during a normal operating mode, can nonetheless be selectively "stressed" or tested by an elevated or other stress voltage during a stress mode. This is accomplished by allowing the device to enter a stress mode in response to certain conditions during which the primary function, or protected, circuit is supplied with an elevated or other voltage in order that it might be subjected to stress testing. (pages 1-2, 4, 15 of the specification). Acceptable conditions for entry of the device into the stress mode may include the external voltage supplied to the device being outside a predetermined, acceptable range (such as being above a prescribed maximum or below a normal voltage range) or by supplying a control signal to the device (pages 2, 4, 15 of the specification). In a first embodiment, the use of an optional voltage detector of the voltage regulator detects whether the externally supplied voltage is outside the acceptable range and generates a stress-enable signal indicative of the state of the externally supplied voltage. Alternately, the stress-enable signal may be supplied externally to the device via a connector or pin (page 5 of the specification).

Contrast this with the teaching of the Basso et al. reference. In Basso, there are two modes of operation taught, the linear and switched modes of operation, and which mode is realized is a function of the load conditions experienced at Vout, shown in FIGs. 1 and 2. Selection of the proper mode, whether it be the switched mode in which pulse width modulation techniques are used or the linear mode during which

linear conversion techniques are used, allows for the adjustment of the duty cycle of a drive signal in response to the power requirements of the load. As noted at column 3, lines 7-40:

> During switched mode operation, buck voltage converter 18 adjusts the duty cycle of a gate drive signal of an internal transistor according to the power requirements of the load. As the load at terminal Vout requires less power, the voltage at terminal Vout increases above some predetermined threshold and the duty cycle of the gate drive signal is decreased. Decreasing the duty cycle of the gate drive signal also decreases the amount of time that capacitor 12 is being charged during a charging cycle of buck voltage converter 18. Increasing the duty cycle of the gate drive signal also increases the amount of time that capacitor 12 is being charged during a charging cycle of buck voltage converter 18. A duty cycle, therefore, is associated with the gate drive signal as being the ratio of time when the capacitor 12 is being charged to the time that the capacitor 12 is discharging during one charging cycle in a switched mode of operation. Buck voltage converter 18 adjusts the duty cycle of the gate drive signal between a minimum and a maximum value while buck voltage converter 18 is programmed for switched mode operation based on an internal feedback signal developed within buck voltage controller 18.
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> Conversely, micro-controller 288 senses inactivity within transceiver 24 during a stand-by mode of operation whereon communications are taking place. Under low load, the power required by baseband block 22 reduces below the minimum power that can be produced by buck voltage converter 18 during the switched mode of operation. Micro-controller 28 senses the stand-by mode through signal LOAD SENSE and signals buck voltage converter 18 to a linear mode of operation via the MODE terminal. Micro-controller 28 programs buck voltage regulator 18 to a linear mode of operation by removing the mode signal at terminal MODE...."

From these descriptions, it can be seen that there are at least several differences between the claimed invention and the Basso et al. reference. First, in the claimed invention, the voltage regulator is operative to protect the primary-function circuit, of which the voltage regulator is internal, from voltages that fall outside a predetermined range. In Basso et al., the function of the buck voltage converter 18

is to operate in either a switched mode or a linear mode, as determined by the load conditions experienced by baseband block and evidenced at Vout, in order to be more power efficient. This difference is understood by a reading of the application and the reference. Moreover, Applicant's specification makes the purpose of voltage regulator 101 clear. Applicant has amended independent claims 1 and 13 to make this implicit meaning of the claims clear.

Second, in the claimed invention the two modes are normal and stress mode. In the normal mode, the voltage regulator performs its normal job of protecting the primary-function circuit from over/undervoltage conditions by supplying only those voltages to the primary-function circuit that are within an acceptable predetermined range. This contrasts with the Basso et al. reference in which the two modes, switched and linear, are determined not by the voltage level being supplied the buck voltage converter but by the load experienced at Vout, as explained above. Applicant has amended the independent claims to make clear these modes of operation.

Third, the subject claims recite that the primary function circuit and the voltage regulator are integrated in the electronic device. This, as described in the specification, allows the voltage regulator to protect the primary function circuit from undesirable (i.e. test) voltage conditions during normal operation. This is not envisioned, taught, suggested or otherwise anticipated by Basso et al., not in the least due to the fact that Basso et al. is not concerned with protecting a circuit from errant voltage conditions in certain modes. It is important to note that independent claims 1 and 13 both recite this aspect of the claimed invention; claim 1 recites that they are integrated in the electronic device and claim 13 recites "an electronic device having an integrated voltage regulator..."

For the foregoing reasons, Applicant respectfully submits that this rejection of the claims has been overcome. Reconsideration and allowance of claims 1, 2, and 13-15 is earnestly solicited at the examiner's earliest convenience.

Claim Rejections 35 USC §103

The Examiner has rejected Claim 3 under 35 U.S.C. 103(a) as being unpatentable over Basso et al. in view of Pangal et al. Applicant respectfully traverses this rejection of Claim 3. This claim depends from claim 1, which, as described at length above, is believed to be patentably distinct over the reference cited against it. It must be noted that combining the Pangal et al. reference with Basso et al. does not cure the shortcomings noted above, nor was the Pangal et al. reference relied upon for this purpose. Reconsideration and allowance of claim 3 is therefore earnestly requested at the examiner's earliest convenience.

Allowable Subject Matter

Applicant notes with appreciation that claims 4-12 and 16-20 are objected to but would be allowable if rewritten in independent form. While Applicant agrees that these claims define patentable subject matter in their own right, it is also believed that the claims from which they depend are patentable as well for the reasons set forth above. Applicant therefore respectfully declines to amend these claims into independent form at this time but does reserve the right to do so if necessary at a later time during prosecution of this application.

For the foregoing reasons, Applicant respectfully submits that all pending claims of the instant applicant are allowable over the art of record. Reconsideration and allowance of the claims is hereby requested at the Examiner's earliest convenience. Please contact the undersigned if there are any questions regarding this response or application.

Respectfully submitted,

Renee' Michelle Leveque
Registration No. 36,193
Leveque IP Law, PC
221 East Church Street
Frederick, MD 21701
Phone (301) 668-3073